International Journal of Engineering & Scientific Research
Vol.4 Issue 10, October 2016,
ISSN: 2347-6532 Impact Factor: 5.900
Journal Homepage: http://www.ijmra.us, Email: editorijmie@gmail.com
Double-Blind Peer Reviewed Refereed Open Access International Journal - Included in the International Serial Directories Indexed & Listed at: Ulrich's Periodicals Directory ©, U.S.A., Open J-Gage as well as in Cabell's Directories of Publishing Opportunities, U.S.A

DGMOSFET CAPACITANCE MODELLING AND VERILOG-A IMPLEMENTATION OF MODEL

Monika Chaudhary[*]
Varun Mehta*
Er. Deepti Garg (Research Supervisor)*

ABSTRACT:

In this work we present the model based on analytical solution of highly symmetric Double-gate (DG) MOSFET that aims at giving a comprehensive understanding of the device for design strategy. An explicit solution to implicit algebraic equations with high accuracy has been developed. The model is derived from closed form solution of Poisson's equation and without charge sheet approximation. The drain current, transconductance and capacitances are written as explicit intermediate parameter. The entire Ids(V_g, V_{ds}) characteristics for all the regions of MOSFET operation: linear, saturation and subthreshold are covered under one continuous function, making it ideally suited for compact modeling in an optimized fashion.

---

[*] Dept of Electronics and Communication Engineering, YIET, Gadholi,Yamuna Nagar Haryana

INTRODUCTION

A circuit simulation model of a DGMOSFET is developed using Verilog-A (hardware description language) [1] .Capacitance-voltage (*C*–*V*) and current-voltage (*I*–*V*) characteristics are simulated in Spectre circuit simulator within Cadence CAD system and verify the accuracy of the proposed analytical model with TCAD simulation results [2] .

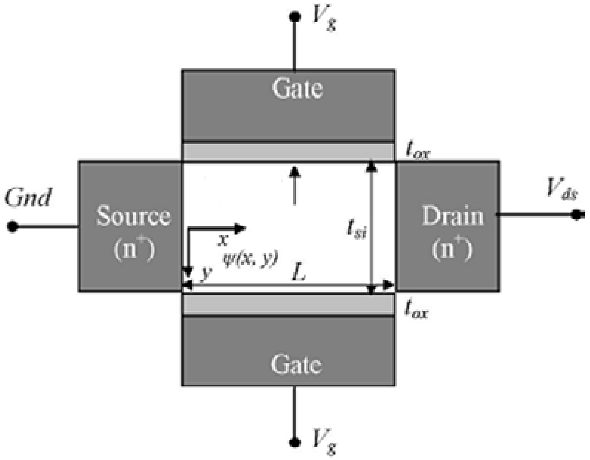

Fig1: Schematic diagram of symmetric DG N-MOSFET

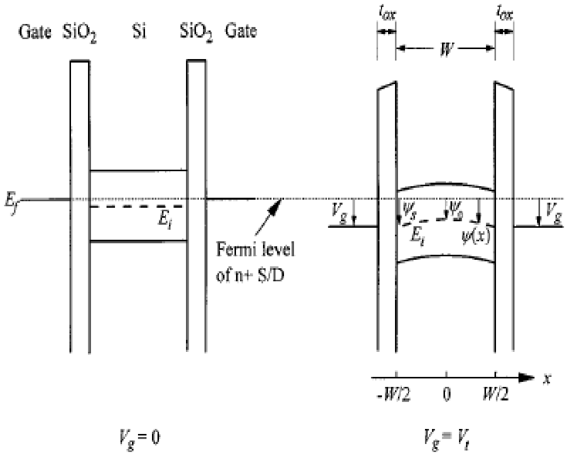

Fig2. Schematic band diagram of symmetric DG N-MOSFET

In bulk MOSFET, the starting point is Pao-Sah integral based on poisson's equation and current continuous equation with gradual channel approximation [3]. An analytic potential model for symmetric double gate (DG) MOSFETs was first derived by solving Poisson and current continuity equations with the gradual channel approximation in terms of an intermediate parameter (β). Current and capacitance analytical model are derived further in terms of same intermediate parameter (β). Even far less work has been done on charge and capacitance modeling of these devices; however analytical charge and capacitance models are much more suitable for circuit simulation (delay, rise/fall time) [4] .

DGMOSFET Modelling

Considering a symmetric doped or undoped DGMOSFET shown in the fig .1 Poisson's equation along vertical cross section of si film takes the following form with mobile charge as electrons only [5].

$$\frac{d^2\Psi}{dx^2} = \frac{q}{\varepsilon_{si}} n_i e^{\frac{q(\Psi - V)}{kT}} \qquad (1)$$

Since the current flows predominantly from the source to the drain along the y-direction, the gradient of the electron quasi-Fermi potential is also in the y-direction [6]. Solved with boundary condition

$$\frac{V_g - \Delta\emptyset - V}{V_t} - \ln\left[\frac{2}{t_{si}}\sqrt{\frac{\varepsilon_{si} V_t}{q n_i}}\right] = ln\,\beta - \ln[cos\beta] + 2r\beta tan\beta \qquad (2)$$

Here we used newton raphson method for feasible values of β i.e. $0<\beta<\pi/2$

$$\mathrm{I_{ds}} = \mu \frac{\mathrm{W}}{\mathrm{L}} 4\, C_{si} \mathrm{V_t}^2 \times \left[\beta tan\beta - \frac{\beta^2}{2} + r(\beta tan\beta)^2\right]_{\beta_d}^{\beta_s} \qquad (6)$$

Where where β_s and β_d are the solution of (4) correspond to the V=0 and $V=V_{ds}$ respectively.

Capacitance model can be given as [7]

$$C_g = -\frac{L^2 {g_{ds}}^2}{\mu I_{ds}} + \frac{Q_g g_{ds}}{I_{ds}} \qquad (3)$$

Above derived equations are derived analytically and implemented in Verilog—A and results are compared with TCAD simulations results [8-10]

Conclusion

Double gate MOSFET saves the transistor count of the network. It operates at lower voltages than present CMOS devices. Stability is at lower voltage.

Proposed Future Work

To Implement the DG-MOSFET for analog and digital applications and study and compare its behavior with conventional MOSFETs

References

[1]. Verilog-A language reference Manual. Version 1.0. Open Verilog International 1996.

[2]. G. Recktenwald. Numerical Methods with Matlab. Prentice Hall, 2000.

[3]. PSP. http://pspmodel.asu.edu/introduction.htm.

[4]. Spectre.http:www.cadence.com/products/rf/spectrecircuit/pages/default.aspx

[5]. Designer's Guide Community. http://www.designers-guide.org/.

[6]. K. K. Young, "Analysis of conductionin fully depleted SOI MOSFETs", *IEEE Trans. Electron Devices*, vol. 36, pp.504 -506, 1989.

[7]. H. C. Pao and C. T. Sah, “Effects of diffusion current on characteristics of metal-oxide (insulator)—semiconductor transistors,” *Solid-State Electron.*, vol. 9, pp. 927, 1966.

[8]. K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, and Y. Arimoto, "Scaling theory for double-gate SOI MOSFETs", *IEEE Trans. Electron Devices*, vol. 40, pp.2326 -2329, 1993.

[9]. J. P. Colinge, M. H. Gao, A. Romano-Rodriguez, H. Maes, and C. Claeys, "Silicon-on-insulator gate-all-around device," *International Electron DevicesMeeting (IEDM)*, pp. 595-598, 1990.

[10]. J.T. Park, J. P. Colinge, and C. H. Diaz, "Pi-Gate SOI MOSFET," *Electron DeviceLetters, IEEE*, vol. 22, pp. 405-406, 2001.